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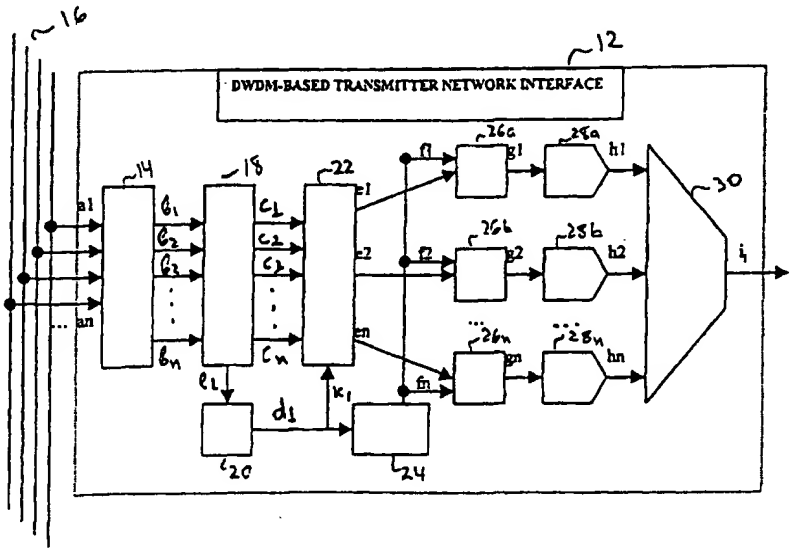
(54) Title: DENSE WAVELENGTH DIVISION MULTIPLEXING–BASED NETWORK INTERFACE MODULE

(57) Abstract

A DWDM–based network interface module connects directly to the internal bus (or switch) core of a communications system via a standard integrated bus–bridge to provide low latency transmission (via multiple 'virtual' DWDM channels) and interconnect speeds in excess of 10 Gbps over a range of about two hundred kilometers. Depending on directional transmission capability (transmitter, receiver or transceiver), the network interface may include a data buffer unit, a clock generator, a time division multiplexing unit, a channel ID generator or a channel ID verifier, a data encoder/scrambler or a data decoder/unscrambler, a data sequencer/reshaper, a DWDM transmitter and a DWDM multiplexer, or a DWDM receiver and a DWDM demultiplexer, or both, and a directional optical coupler. The direct bus/switch connection bypasses any MAC (Media Access Control) layer buffering and allows two switch chipsets to connect as a single device across a core bus (such as PCI). Multiple chips distribute switching loads and directly communicate with their counterparts at the speed of the bus, which far exceeds the conventional interconnect speed via I/O ports, eliminating all buffering and interface costs normally associated with high speed aggregation. The network interface module transports physical bus or switch signals via a plurality of DWDM channels creating in effect a virtual device that extends from a few meters to over hundreds of kilometers.



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DENSE WAVELENGTH DIVISION MULTIPLEXING-BASED NETWORK INTERFACE MODULE

BACKGROUND OF THE INVENTION

This application claims the benefit of United States Provisional Application Serial No. 60/131,725, filed April 30, 1999.

Field of the Invention

The present invention relates generally to communication systems and more particularly to data and optical telecommunication systems which carry multi-channel information across optical network interfaces.

Prior Art

Telecommunications and data communication systems represent a substantial and rapidly growing portion of the communications industry. Such growth has been particularly intense in the past ten years. While the total internal switching and routing capacity of these systems has grown exponentially in the past few years, networking protocols have not kept pace with the capacity growth, limiting the speeds at which telecommunication devices interconnect with one another. Various methods have been utilized to increase system capacity, such as frequency division multiplexing (FDM), time division multiplexing (TDM) and wavelength division multiplexing (WDM).

Frequency division multiplexing is characterized by subdivision of the available bandwidth into bands of sub-frequencies. Each of these sub-frequency bands is dedicated to a specific user and remains permanently dedicated and, therefore, unavailable for use by other users even when a particular sub-frequency band is in an idle state which makes for an inefficient transmission operation. In a fiber optic FDM system, a particular sub-carrier frequency is assigned to each signal source, and a complete signal is constructed by combining the sub-carrier frequencies. The capacity of an FDM system is limited by the need for high signal-to-noise ratio which requires the use of high-power systems which in turn limits the number of data channels due to interference, cross talk and nonlinearity of the optical waveguide medium due to inadequate separation of channels.

Time division multiplexing is characterized by division of the available bandwidth into time slices (slots). A communicating device can dominate the entire bandwidth for the duration of a time slot. These slots are shared according to an algorithm and if a station does not need to transmit, its time slot is automatically allocated to another station that needs to transmit. This type resource allocation optimizes the use of the transmission facility's entire available bandwidth. However, time division multiplexing has an inherent overhead cost due to the need to maintain synchronization at all times. If synchronization is lost, the transmitted data may become corrupted. In a fiber optic TDM system, the use of a single optical channel (fiber optic strand) is rotated between various signal sources with a portion of one signal transmitted, followed by a portion of another and in which complete signals are constructed from the portions of signals collected from each time slot. The capacity of such a system is limited by the speed

of electronic switching between time slots which translates into a limited optimal data transfer rate.

In a fiber optic WDM system, multiple optical signal channels are carried over a single waveguide (fiber optic strand) with each channel being assigned a particular wavelength.

Traditionally, time division multiplexed (TDM) network interfaces have been used to network high-speed communication systems. In recent years, a new technology has emerged, namely dense WDM, as an alternative to higher speed TDM systems. Dense WDM was introduced to increase the bandwidth of a WDM system whereby a so-called dense WDM (DWDM) standard has been proposed in which channel separation of signals is set at 0.8 nm in wavelength or 100 GHz in frequency which substantially increases the number of available data carrying channels.

Dense wavelength division multiplexing is the process of multiplexing signals of different wavelengths onto a single optical fiber which results in the creation of a great number of virtual fibers each capable of carrying a different signal. At its simplest, a DWDM system incorporates a set of parallel optical channels with each channel using a slightly different light wavelength over a single transmission medium. This type of setup significantly increases the capacity of existing networks without the need for expensive re-cabling and also reduces the cost of future network upgrades. Since an optical fiber can transmit in both directions, a DWDM system can be implemented as a uni- or bi-directional system depending on the needs of the user. A DWDM system typically includes optical amplifiers (usually Erbium-doped fiber amplifiers), wavelength converters, wavelength add/drop multiplexers and optical cross connect units. Such a system can gather signals from a variety of sources such as voice, video, internet server and the like and

transmit the signal simultaneously from one location to another. A demultiplexer unit at the other end of the fiber separates the different signals and sends the same to their receiving locations. A DWDM system can also be used to segregate groups of users or services onto individual bandwidths making high-bandwidth networks easier to manage and/or maintain. Network providers can lease "secure" wavelengths on their networks or provide optical add/drop multiplexing and routing for more reliable and manageable networking.

By using a single fiber to carry multiple transmission channels, DWDM has been established as an efficient approach for aggregating the output of multiple interfaces of one or more communication systems and for increasing the utilization of the existing transmission medium (optical fiber).

Currently, 2.5 Gbps network interfaces are common and 10 Gbps interfaces are about to become the new standard for a high-speed optical channel. As communications systems reach internal capacities in excess of 100 Gbps, it is becoming apparent that even a 10 Gbps network interface will not provide sufficient capacity to interconnect multiple high-speed communication systems. Presently, TDM signals at data rates in excess of 10 Gbps are not cost-effective or commercially viable, while communication systems with internal capacity exceeding 1000 Gbps (1Tbps) are beginning to appear in the telecommunications market.

Even if TDM technology could be scaled to higher speeds, another problem with the current generation of network interfaces is that the vast majority of network interfaces requires extensive data queuing and packetization at each interface. For instance, with networking protocols like Ethernet, ATM (Asynchronous Transfer Mode) and SONET (Synchronous Optical Network), all data is organized into packets and typically an entire packet of data must

be queued at the transmitting interface which provides a source of latency for the entire network. Even in devices that attempt to minimize this interface latency (cut-through switches), dozens of bytes must still be queued before transmission begins. At the receiver end, the packetized information is queued in incoming buffers, until the entire packet is received. Once an entire packet is received, it can then be processed. Nowadays, when networks are being deployed with capabilities for real-time voice, video and data services, such inherent sources of latency can be a constant source of problem for the network provider and user.

Modern technology is capable of providing interconnections at far greater data rates, but the interconnection range has been generally limited to a distance of a few meters or less. Typically, an interface directly connected to the internal bus or switch core would electrically bridge the same and extend the internal bus/switch core range to a few meters. These "bus-bridges" can be used to connect multiple physical devices into a single logical or "virtual" device. The resulting virtual device operates at the internal speed of the bus or switch core minimizing the interconnection latency. Specifically, with regard to the internal bus/interface connection, there are bus extenders on the market today that are capable of extending an internal bus by not more than a few meters or so.

With some lower-speed LAN (Local Area Network) and WAN (Wide Area Network) technologies, standards have been developed that treat a combination of physical interfaces as a single logical interface. Examples of such an approach are the bonding of multiple modems together (multi-link point-to-point protocol [PPP]) or the bonding of multiple Fast Ethernet interfaces together (Fast EtherChannel). The goal in both cases is to create a single connection between systems that has a higher aggregate data rate than a single unbonded channel.

With the introduction of high-speed Internet access devices (xDSL, cable modem), the need arises to aggregate a large enough number of ports to make the overall system cost effective. For example, a DSL implementation may use Ethernet at the remote site as the basic network access protocol with the remote device having Ethernet-to-ATM routers with the front end converting the ATM cells to HDLC (High Level Data Link Control) for transmission to the local POP (points of presence). The DSL switch converts from HDLC back to ATM, uses an ATM switch to further aggregate before finally converting to SONET to interface with the carrier backbone. Each conversion introduces cost and latency which is undesirable for the network service provider.

Various new transport standards such as IP (Internet Protocol) over SONET are currently in development. Traditional SONET technology is, however, relatively costly and not available at speeds greater than OC (Optical Carrier)-48 which corresponds to 2.488 Gbps. In this regard, the only viable medium today to interconnect two Gigabit Ethernet switches is SONET OC-48 which means that the hardware must convert at gigabit speeds between the raw Ethernet format and the SONET framing format. This type of set up is not only relatively costly as it requires extensive frame buffering, but it only works at speeds up to 2.5 Gbps. Multiple SONET pipes require multiple fiber runs which leads to a cost-prohibitive setup for the network provider. Moreover, SONET is not particularly well suited to handle protocols such as Switched Fast Ethernet, Gigabit Ethernet, FDDI (Fiber Distributed Data Interface), ESCON (Enterprise System Connection), HIPPI (High Performance Parallel Interface) and various digital audio and video formats.

A "transparent" DWDM transport standard has been proposed by the assignee of the instant application which keeps the data in its native format, based on the underlying technology disclosed in International PCT Publication No. WO 99/35775, published on July 15, 1999, International PCT Publication No. WO 99/41863, published on August 19, 1999 and International PCT Publication No. WO 99/52232, published on October 14, 1999 with all three PCT publications incorporated herein by reference.

However, there is still a need for a novel high-speed network interface which can reliably and efficiently link two or more communication systems at scalable speeds in excess of 10 Gbps. Such a novel network interface should connect directly to the communication system's internal bus/switch core and preferably incorporate the DWDM networking technology disclosed in the above-identified PCT publications to provide extremely low latency throughput. The inventive network interface should also be modular and adaptable. It must be expandable while maintaining existing traffic flow and it must adhere to a pay-as-you-grow philosophy to allow incremental add-ons when network capacity requirements increase. Due to the current diversity of network requirements, such an interface should also be format and bit-rate transparent to allow the service provider to quickly adjust to changing data types and/or services being provided. A network interface of this type should also be cost-efficient to manufacture and install in view of the ever-increasing costs for laying down new fiber optic lines. Furthermore, all of the discrete components of the novel network interface should preferably be merged into an embedded module that can fit directly into the end user's equipment.

SUMMARY OF THE INVENTION

The present invention is directed to a dense wavelength division multiplexing-based transmitter network interface module for coupling the internal bus/switch core backplane of a personal computer or other node of a communication system to at least one optical fiber trunk, the dense wavelength division multiplexing-based transmitter network interface module comprising a bus/switch bridge electrically coupled directly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane; a data buffer coupled electrically to the bus/switch bridge for buffering information transmitted from the bus/switch core backplane through the bus/switch bridge between bus cycles and generating electrical output signals; a time division multiplexing unit coupled electrically to the data buffer for receiving the electrical output signals and outputting one or more electrical time division multiplexed output signals; at least one dense wavelength division multiplexing transmitter for receiving the multiplexed electrical signals and generating one or more narrowband dense wavelength division multiplexing optical signals; and a dense wavelength division multiplexing multiplexer optically coupled to the dense wavelength division multiplexing transmitters for receiving the narrowband optical signals and optically multiplexing the narrowband optical signals for output onto the optical fiber trunk in their native format.

The present invention is also directed to a dense wavelength division multiplexing-based receiver network interface module for coupling at least one optical fiber trunk to the internal bus/switch core backplane of a personal computer or other node of a communication system, the dense wavelength division multiplexing-based receiver network interface module comprising

a bus/switch bridge electrically coupled directly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane; a dense wavelength division multiplexing demultiplexer optically coupled to at least one optical fiber trunk for receiving a dense wavelength division multiplexed optical signal from the at least one optical fiber trunk and separating the received dense wavelength division multiplexed optical signal by wavelength into one or more individual optical output signals; one or more dense wavelength division multiplexing receivers optically coupled to the dense wavelength division multiplexing demultiplexer for receiving the individual optical output signals and converting the received individual optical output signals into corresponding electrical output signals; and a time division demultiplexing unit for reconstructing the received electrical output signals in their native format.

One or more of the transmitter network interface modules and one or more of the receiver network interface modules may be combined to form a unidirectional or bidirectional or ring communication network connecting the internal bus/switch core backplanes of two or more network nodes.

A method for extending the bus/switch core of a communication system over a substantial distance is also disclosed. The novel method includes the steps of:

(a) providing at least two dense wavelength division multiplexing-based network interface modules, each having at least one bus/switch bridge,

(b) electrically coupling the first bus/switch bridge directly to a bus/switch core backplane of the communication system; and

(c) electrically coupling the second bus/switch bridge directly to the bus/switch core backplane of a second communication system,

(d) using a wavelength division optical fiber and a combination of dense wavelength division optical multiplexing and time division electrical multiplexing to connect the first bus/bridge to the second bus/bridge,

wherein the optical multiplexing and the electrical multiplexing is transparent to the native format of the electrical signals received from and transmitted to the bus/switch bridges.

Preferably the dense wavelength division multiplexed optical fiber trunk is sufficiently short and has only minimal attenuation and dispersion to facilitate the use of direct optical modulation in the optical transmitters without any amplification or regeneration between the transmitter and the receiver.

In accordance with other, more specific aspects of the invention, the individual electrical signals may be coded, scrambled, sequenced and/or shaped as part of the multiplexing process, in order to facilitate reconstruction into their native format.

These and other aspects of the present invention will become apparent from a review of the accompanying drawings and the following detailed description of the preferred embodiments of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a communication network including a pair of integrated fiber optically connected DWDM-based transceiver network interface modules for bidirectional information transmission in accordance with the present invention;

Figure 2 is a block diagram of an integrated DWDM-based transmitter network interface module directly connected to the internal bus/switch core of a communication system in accordance with the present invention;

Figure 3 is a block diagram of an integrated DWDM-based receiver network interface module directly connected to the internal bus/switch core of a communication system in accordance with the present invention;

Figure 4 is a block diagram of an integrated DWDM-based transceiver network interface module directly connected to the internal bus/switch core of a communication system in accordance with the present invention; and

Figure 5 is a schematic representation of a ring topology network comprising four optically interlinked communication systems with each communication system incorporating a pair of integrated DWDM-based transceiver network interface modules for unidirectional or bidirectional fiber optic transmission in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, some preferred embodiments of the present invention will be described in detail with reference to the related drawings of Figures 1 - 5. Additional embodiments, features and/or advantages of the invention will become apparent from the ensuing description or may be learned by the practice of the invention.

The following description includes the best mode presently contemplated for carrying out the invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention.

The present invention refers to a DWDM-based network interface module which connects directly to the internal bus (or switch) core of a communications system via a standard bus-bridge to provide low latency transmission (via multiple 'virtual' DWDM channels) and interconnect speeds in excess of 10 Gbps over a range of about two hundred kilometers. The bus-bridge may be an integral part of a DWDM-based transceiver network interface module, a DWDM-based transmitter network interface module or a DWDM-based receiver network interface module. Depending on directional transmission capability, the novel network interface may include a data buffer unit, a clock generator, a time division multiplexing unit, a channel ID generator or a channel ID verifier, a data encoder/scrambler or a data decoder/unscrambler, a data sequencer/reshaper, a DWDM transmitter and a DWDM multiplexer, or a DWDM receiver and a DWDM demultiplexer, or both, and a directional optical coupler. The direct bus connection bypasses any MAC (Media Access Control) layer buffering and allows two switches to connect as a single device. Most of the current generation Ethernet and Fast Ethernet switch chipsets can be interconnected across a core bus (like PCI). Hence, multiple chips can distribute

switching loads and directly communicate with their counterparts at the speed of the bus (with the speed of the bus far exceeding the interconnect speed via the standard I/O ports). The novel network interface transports physical bus or switch signals via a plurality of DWDM channels creating in effect a virtual device that extends over hundreds of kilometers. Even with signal propagation delays, latency in such a virtual device is estimated to be generally less than a millisecond. For example, a standard PCI-to-PCI bus bridge may be used as part of the novel network interface to interconnect separate Fast Ethernet switches across a gigabit bus. The switches would detect each other on the gigabit bus and would transfer data at bus speeds between the Fast Ethernet switch chips. The novel interface is modular, adaptive, can be integrated with the terminal equipment and requires no high-speed ports at all eliminating all buffering and interface costs normally associated with high speed aggregation.

Referring now more particularly to Fig. 1, a DWDM-based transceiver network interface module, generally referred to by reference numeral 2, is shown electrically connected to an internal bus/switch core backplane 4. Transceiver network interface module 2 includes a DWDM transmitter, a DWDM receiver, a DWDM multiplexer, a DWDM demultiplexer and an optical directional coupler which interfaces with an optical fiber cable 6. The function of the transmitter portion of transceiver network interface module 2 is to receive electrical input signals (r_1, r_2, r_3, r_4, etc.) from internal bus/switch core backplane 4 and convert the same to a narrowband optical signal suitable (multiplexed) for transport over optical fiber cable 6. Electrical input signals (r_1, r_2, r_3, r_4) may be telecommunication or data signals in virtually any format, such as standard or proprietary bus architectures, interfaces to switch fabrics, or other backplane interfaces and may include both data signals, addressing signals and additional

bus/switch control signals that must be passed across the interface. Optical fiber 6 is capable of carrying multiplexed optical signals in their native format in both directions to/from a counterpart DWDM-based transceiver network interface module 8 which is respectively electrically connected to an internal bus/switch core backplane 10. Transceiver network interface module 8 also includes a DWDM transmitter, a DWDM receiver, a DWDM multiplexer, a DWDM demultiplexer and a counterpart optical directional coupler which interfaces with optical fiber cable 6. The function of the transmitter portion of transceiver network interface module 8 is to take electrical input signals (r_1', r_2', r_3', r_4', etc.) (which may be of the same type as electrical input signals (r_1, r_2, r_3, r_4, etc.)) from an internal bus/switch core backplane 10 and convert the same to a narrowband optical signal suitable (multiplexed) for transport over optical fiber cable 6 to transceiver network interface module 2. The function of the receiver portion of transceiver network interface module 2 is to receive the incoming multiplexed optical signal from optical fiber 6 (which is sent by the transmitter portion of transceiver network interface module 8) and convert the same to a series of electrical output signals (r_1, r_2, r_3, r_4, etc.) suitable for output to internal bus/switch core backplane 4. Similarly, the function of the receiver portion of transceiver network interface module 8 is to receive the incoming multiplexed optical signal from optical fiber 6 (which is sent by the transmitter portion of transceiver network interface module 2) and convert the same to a series of electrical output signals (r_1', r_2', r_3', r_4', etc.) suitable for output to internal bus/switch core backplane 10. The internal architecture of a transceiver network interface module such as transceiver network interface modules 2, 8 constructed in accordance with the general principles of the present invention is shown in Fig. 3.

Figure 2 illustrates the internal architecture of a DWDM-based transmitter network interface module 12. In accordance with a preferred embodiment of the present invention, transmitter module 12 comprises a standard bus/switch bridge 14 which is electrically coupled to an internal bus/switch core backplane 16 and isolates bus/switch core backplane 16 from the rest of the system. Bus/switch bridge 14 receives electrical input signals (a_1,... a_n) from backplane 16 and preferably includes logic components to isolate the local bus/switch core backplane 16 from erroneous information that could arrive from remotely attached communication systems (e.g. due to cable faults, component failures or other bit or system errors). It is also desirable, although not mandatory that bus/switch bridge 14 be constructed to allow for transparent and asynchronous operation (both sides of bus bridge 14 operate autonomously and asynchronously). If electrical signals are destined for the local side of the bus, such signals are not bridged to the other side of bus/switch bridge 14. Only those signals that are destined for a remote location are actually bridged across bus/switch bridge 14 to ensure optimal utilization of resources on both sides of bus/switch bridge 14.

An example of a standard bus bridge that is suitable for use in accordance with the present invention is Intel's 21154 PCI-to-PCI bus bridge which provides a connection between two independent PCI buses. The 21154 bus bridge may be implemented on a system backplane to provide capability for additional slots and devices and operates at 64x66 MHz (4Gbps). The 21154 bus bridge is a transparent device, that is, it requires no special driver software to run in a system and allows the two PCI buses to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy. This type of traffic isolation enhances system performance in various telecommunication applications. It should be

appreciated by a person skilled in the art that proprietary buses and switches may also be accommodated provided that compatible custom bus/switch bridges are provided.

Transmitter network interface module 12 further comprises a data buffer 18 which receives electrical input signals (b_1, b_2, b_3, ..., b_n) and preferably includes sufficient buffering capability to buffer information for the longest possible delay between bus cycles. Sufficient buffering ensures that data will not be lost between two or more communication systems due to round trip delays in transmitting request signals and receiving reply signals across the longest links. Although parallel input signals (b_1, b_2, b_3, ..., b_n) are shown between bus/switch bridge 14 and data buffer 18, in practice the bus/switch bridge and the data buffer may be a single integrated physical device.

Other components of transmitter network interface module 12 include a clock generator 20 which supplies timing information (signal k_1) to a TDM (time division multiplexing) unit 22 as well as (signal d_1) to a channel ID generator 24. Clock generator 20 receives electrical input (signal l_1) from data buffer 18 and generates a main system clock, in the form of synchronous pulses based on the speed of the input signal to control time division multiplexing unit 22.

Time division multiplexing unit 22 combines electrical input signals (c_1, c_2, c_3, ..., c_n) from data buffer 18 by sequentially picking up each input signal and producing one or more output signals (e_1, e_2, ... , e_n). Multiplexing may be done in any reasonable manner with the most obvious being to take each input signal and duplicate it as the output signal for one channel in a one-to-one fashion using a single integrated device. Other multiplexing schemes may be utilized provided such schemes do not depart from the intended purpose of the present invention.

Channel ID generator 24 generates a series of unique channel ID signals (f_1, f_2, ... , f_n) for the marking of each channel respectively by the data encoder portion of data encoders/scramblers (26_a, 26_b, ... , 26_n) which receive input channel ID signals (f_1, f_2, ... , f_n) (Fig. 2). Typically, this is in the form of unique pseudo-random numbers (between 0 and 127) which are sent to each data encoder (26_a, 26_b, ... , 26_n). The numbers may be stored in a shift register or ROM (read-only memory) or the like by channel ID generator 24. For instance, channel ID signal f_1 is sent to data encoder 26_a, channel ID signal f_2 is sent to data encoder 26_b, etc. In another preferred embodiment of the present invention, the data encoder (26_a, 26_b, ... , 26_n) will insert one bit of the pseudo-random number every eight bits of the data buffer's output (c_1, c_2, c_3, ..., c_n). It should be appreciated by a person skilled in the art that channel ID generator 24 must be selected such that the relationship between the plurality of channels can be determined at the network receiver end. The basic function of the data encoder is to add an identification signal supplied by channel ID generator 24 to the terminal signal. Suitable channel ID generators are commercially available from electronic manufacturers such as Motorola and National Semiconductor.

Data encoders/scramblers (26_a, 26_b, ... , 26_n) also receive input signals (e_1, e_2, ... , e_n) from TDM unit 22 as shown in Figure 2. In accordance with the best mode for practicing the invention, as each signal is re-encoded to include the identification signal, it is also scrambled to alter the output of the encoders according to a preset algorithm so as to avoid unrecognizable data. Suitable data scramblers are commercially available from suppliers like Motorola and National Semiconductor. It should be appreciated by a person skilled in the art that if desired, additional information may be added to the data encoding process to improve the reliability of

the decoded signal. For example, commercially available forward error correcting (FEC) codes may be utilized to improve the signal integrity at the network receiver even in the presence of certain bit errors.

The data scrambler portion of data encoders/scramblers (26_a, 26_b, ... , 26_n) utilizes an Exclusive OR algorithm based on a different binary number for each data scrambler. The binary numbers must be of sufficient length and diversity to assure that they will not be duplicated in the data buffer's output. It has been found that a 7-bit binary number is usually adequate for this purpose. The binary and exclusive OR algorithm (as well as the necessary output hardware) can be impressed upon a single chip which can also be used to unscramble the data at the network receiver. Thus, the data scrambler will avoid data recognition problems caused by null signals (repeating zeros) as well as other signals (repetitive 1's, "001100110011...", etc.) where the signal horizon is relatively difficult to determine.

Optionally, data encoders/scramblers (26_a, 26_b, ... , 26_n) may also include data framers, (such as SONET or SONET-like protocols), so that each individual channel may be passed transparently across networks that do not recognize the novel DWDM-based network interfaces. Using an optional data framer may increase inter-operability of the optical signals at the expense of somewhat increased latency on the DWDM-based network interface of the present invention.

Another component of transmitter network interface module 12 includes one or more DWDM transmitters (28_a, 28_b, ... , 28_n) which receive electrical input signals (g_1, g_2, ... , g_n) from data encoders/scramblers (26_a, 26_b, ... , 26_n) and generate narrowband DWDM optical output signals (h_1, h_2, ... , h_n) as shown in Figure 2. A variety of DWDM transmitters suitable for use

in accordance with the principles of the present invention are commercially available from a number of sources such as Osicom Technologies, Inc. of San Diego, California.

In accordance with yet another preferred embodiment of the present invention, optical signals ($h_1, h_2, \ldots, h_n$) are then passed to a DWDM multiplexer 30 which optically multiplexes each individual optical signal onto one or more optical fiber trunks. A variety of DWDM multiplexers are commercially available from a number of sources, including Osicom Technologies, Inc. of San Diego, California. The DWDM multiplexed signal i_1 is then passed through an optical waveguide medium such as optical fiber 6 (of Fig. 1) which transports the multiplexed signal i_1 to a counterpart DWDM-based receiver network interface.

The following example further illustrates the novel network interface. A standard PCI bus (such as one used in a personal computer [PC]) is 32-bits wide and runs at 33 million cycles per second (MHz) which translates to just over 1 billion bits per second. In this case, the input to bus bridge 14 would be 32-bits wide. A person skilled in the art should appreciate that the conversion from a parallel data stream (32x33 MHz) to a serial one which is suitable for input into DWDM transmitters ($28_a, 28_b, \ldots, 28_n$) (1x1.056GHz) can be done at the data buffering stage or at the TDM stage (or at both). For instance, a data buffer may output one byte at a time (8x132MHz), so this completes the first stage of parallel to serial conversion. The TDM unit 22 may take 8x132 input and output 1x1056. In a very high speed system (say 25Gbps), the bus/switch core may be running at very high speeds (128x200). In this case, each optical transmitter (at 2.5Gbps) would only be able to accommodate 12 individual signals in which case ten or more optical transmitters would be needed to handle the load. The TDM unit would have to ensure that 12 signals were converted to a single 2.5Gbps data stream.

Figure 3 depicts the internal architecture of a DWDM-based receiver network interface module 42. Specifically, optical waveguide medium (such as optical fiber 6 of Fig. 1) carries the optically multiplexed signal i_1 (transmitted from DWDM multiplexer 30 of Fig. 2) into a DWDM demultiplexer 60 which separates the signal into individual optical output signals (h_1', h_2', ... , h_n'). The DWDM demultiplexer separates the signals by wavelength, segregating the signals from individual time division multiplexers as well as optical or electronic signals from other sources (not shown). A variety of DWDM demultiplexers are commercially available from a number of sources including Osicom Technologies, Inc. of San Diego, California.

Optical output signals (h_1', h_2', ... , h_n') are received by one or more DWDM receivers (58_a, 58_b, ... , 58_n) which provide the mirror function of DWDM transmitters (28_a, 28_b, ... , 28_n) of Figure 2 by converting the individual optical signals (h_1', h_2', ... , h_n') into their corresponding electrical equivalents, i.e. electrical output signals (g_1', g_2', ... , g_n'). DWDM receivers of this type are commercially available from a number of sources including Osicom Technologies, Inc. of San Diego, California.

Electrical output signals (g_1', g_2', ... , g_n'), in turn, are received by one or more data decoders/unscramblers (56_a, 56_b, ... , 56_n) which provide the mirror function of data encoders/scramblers (26_a, 26_b, ... , 26_n) of Figure 2. In the optional case where each incoming electrical signal has been framed, an unframer (not shown) removes the framing information from the incoming electrical signals (g_1', g_2', ... , g_n'). The output from decoders/unscramblers (56_a, 56_b, ... , 56_n) includes electrical decoded data signals (e_1', e_2', ... , e_n') separated from electrical channel ID information signals (f_1', f_2', ... , f_n'). Data signals (e_1', e_2', ... , e_n') are passed to a data resequencer/reshaper 52 while channel ID information signals (f_1', f_2', ... , f_n')

are passed respectively to a channel ID verifier 54 in which the incoming sequencing information is recovered from the channel identification data and passed on to the resequencer portion of resequencer/reshaper 52 in the form of electrical output signal k_1' as shown in Figure 3.

Data resequencer/reshaper 52 receives decoded signals (e_1', e_2', ... , e_n') from data decoders/unscramblers (56_a, 56_b, ... , 56_n) and with sequencing input (signal k_1') from the channel ID verifier 54 constructs a set of electrical output signals (c_1', c_2', ... , c_n') which have been adjusted in phase and frequency. In this regard, depending on the maximum dispersion the system is designed to allow, buffers may be required to compensate for out-of-phase signals.

A clock generator 50 receives electrical input signal d_1' from channel ID verifier 54 and outputs an electrical signal l_1' (Fig. 3). Clock generator 50 derives clocking information from the data resequencer portion of data resequencer/reshaper 52 that is used by a time division demultiplexing unit 48 to reconstruct the original information signal.

In accordance with still another preferred embodiment of the present invention, time division demultiplexing unit 48 provides reconstructed information electrical signals (b_1', b_2', b_3', ..., b_n') to a standard bus bridge 44 which electrically bridges the incoming bus signals onto a bus/switch core backplane 46 via electrical output signals (a_1', a_2', a_3', ... a_n') (Fig. 3) completing the network link. It is also desirable, although not mandatory that bus/switch bridge 44 be constructed to allow for transparent and asynchronous operation (both sides of bus bridge 44 operate autonomously and asynchronously).

It should be further appreciated by a person skilled in the art that DWDM-based transmitter network interface 12 may be coupled via a single optical fiber (not shown) to DWDM-based receiver network interface 42 to establish a one-way traffic link.

A DWDM-based transceiver network interface module, generally referred to by reference numeral 70, is illustrated in Figure 4 in accordance with the general principles of the present invention. Transceiver network interface 70 comprises a DWDM-based transmitter network interface component 80, a DWDM-based receiver network interface component 100 and an optical directional coupler 200 which interfaces with an optical fiber 300. Directional coupler 200 includes an input port 202 for receiving a multiplexed optical output signal 206 from transmitter network interface 80 and transmitting the same to optical fiber 300, an output port 204 for transmitting a multiplexed optical input signal 208 from optical fiber 300 to DWDM-based receiver network interface 100, and an input/output port 210 for communicating with a counterpart transceiver network interface module (not shown) via optical fiber 300. Optical directional couplers of this type may be purchased commercially from a variety of electronics suppliers.

The internal architecture of transmitter network interface component 80 is preferably similar to the internal architecture of transmitter network interface module 12 of Fig. 2 described hereinabove. Specifically, transmitter network interface component 80 comprises a standard bus/switch bridge 84 which is electrically coupled to an internal bus/switch core backplane 86 and isolates bus/switch core backplane 86 from the rest of the system. Bus/switch bridge 84 receives electrical input signals (a_1'',... a_n'') from backplane 86 and preferably includes logic components to isolate the local bus/switch core backplane 86 from erroneous information

that could possibly arrive from remotely attached communication systems (e.g. due to cable faults, component failures or other bit or system errors). It is also desirable, although not mandatory that bus/switch bridge 84 be constructed to allow for transparent and asynchronous operation (both sides of bus/switch bridge 84 operate autonomously and asynchronously). An example of a standard bus bridge that is suitable for use in this embodiment is Intel's 21154 PCI-to-PCI bus bridge which provides a connection between two independent PCI buses. Proprietary buses and switches may be accommodated provided that compatible custom bus/switch bridges are provided.

Transmitter network interface component 80 further comprises a data buffer 88 which receives electrical input signals (b_1'', b_2'', b_3'', ..., b_n'') and preferably includes sufficient buffering capability to buffer information for the longest possible delay between bus cycles. Although parallel input signals are shown between bus/switch bridge 84 and data buffer 88, in practice the bus/switch bridge and the data buffer may be a single integrated physical device.

Other components of transmitter network interface component 80 include a clock generator 90 which supplies timing information (signal k_1'') to a TDM (time division multiplexing) unit 92 as well as (signal d_1'') to a channel ID generator 94. Clock generator 90 receives electrical input (signal l_1'') from data buffer 88 and generates a main system clock, in the form of synchronous pulses based on the speed of the input signal to control time division multiplexing unit 92.

Time division multiplexing unit 92 combines electrical input signals (c_1'', c_2'', c_3'', ..., c_n'') from data buffer 88 by sequentially picking up each input signal and producing one or more output signals (e_1'', e_2'', ... , e_n''). As mentioned hereinabove, multiplexing may be done in any

reasonable manner with the most obvious being to take each input signal and duplicate it as the output signal for one channel in a one-to-one fashion using a single integrated de vice. Other multiplexing schemes may be utilized provided such schemes do not depart from the intended purpose of the present invention.

Channel ID generator 94 generates a series of unique channel ID signals (f_1'', f_2'', ... , f_n'') for the marking of each channel respectively by the data encoder portion of data encoders/scramblers (96_a, 96_b, ... , 96_n) which receive input channel ID signals (f_1'', f_2'', ... , f_n''). The operation of channel ID generator 94 and data encoders/scramblers (96_a, 96_b, ... , 96_n) is as described hereinabove with reference to Figure 2. Data encoders/scramblers (96_a, 96_b, ... , 96_n) also receive input signals (e_1'', e_2'', ... , e_n'') from TDM unit 92 as shown in Figure 4. In accordance with the best mode for practicing the invention, as each signal is re-encoded to include the identification signal, it is also scrambled to alter the output of the encoders according to a preset algorithm so as to avoid unrecognizable data. Additional information may be added to the data encoding process to improve the reliability of the decoded signal. For example, commercially available forward error correcting (FEC) codes may be utilized to improve the signal integrity at the network receiver even in the presence of certain bit errors. The operation of data encoders/scramblers (96_a, 96_b, ... , 96_n) is as described hereinabove with reference to Figure 2. Optionally, data encoders/scramblers (96_a, 96_b, ... , 96_n) may also include data framers, (such as SONET or SONET-like protocols), so that each individual channel may be passed transparently across networks that do not recognize the novel DWDM-based network interfaces.

Another component of transmitter network interface component 80 includes one or more DWDM transmitters (98_a, 98_b, ... , 98_n) which receive electrical input signals (g_1'', g_2'', ... , g_n'') from data encoders/scramblers (96_a, 96_b, ... , 96_n) and generate narrowband DWDM optical output signals (h_1'', h_2'', ... , h_n'') as shown in Figure 4.

In accordance with another preferred embodiment of the present invention, optical signals (h_1'', h_2'', ... , h_n'') are then passed to a DWDM multiplexer 99 which optically multiplexes each individual optical signal onto one or more optical fiber trunks. The DWDM multiplexed signal 206 is then passed an optical waveguide medium to input port 202 of optical directional coupler 200 (Fig. 4).

The internal architecture of receiver network interface component 100 is preferably similar to the internal architecture of receiver network interface module 42 of Fig. 3 described hereinabove. Specifically, optical multiplexed signal 208 from port 204 of optical directional coupler 200 is received by a DWDM demultiplexer 120 which separates the signal into individual optical output signals (h_1''', h_2''', ... , h_n'''). Optical output signals (h_1''', h_2''', ... , h_n''') are received by one or more DWDM receivers (118_a, 118_b, ... 118_n) which convert the individual optical signals (h_1''', h_2''', ... , h_n''') into their corresponding electrical equivalents, i.e. electrical output signals (g_1''', g_2''', ... , g_n'''). Electrical output signals (g_1''', g_2''', ... , g_n''') are received by one or more data decoders/unscramblers (116_a, 116_b, ... , 116_n). In the optional case where each incoming electrical signal has been framed, an unframer (not shown) removes the framing information from the incoming electrical signals (g_1''', g_2''', ... , g_n'''). The output from decoders/unscramblers (116_a, 116_b, ... , 116_n) includes electrical decoded data signals (e_1''', e_2''', ... , e_n''') separated from electrical channel ID information signals (f_1''',

f_2''', ... , f_n'''). Data signals (e_1''', e_2''', ... , e_n''') are passed to a data resequencer/reshaper 112 while channel ID information signals (f_1''', f_2''', ... , f_n''') are passed respectively to a channel ID verifier 114 in which the incoming sequencing information is recovered from the channel identification data and passed on to the resequencer portion of resequencer/reshaper 112 in the form of electrical output signal k_1''' as shown in Figure 4.

Data resequencer/reshaper 112 receives decoded signals (e_1''', e_2''', ... , e_n''') from data decoders/unscramblers (116_a, 116_b, ... , 116_n) and with sequencing input (signal k_1''') from the channel ID verifier 114 constructs a set of electrical output signals (c_1''', c_2''', ... , c_n''') which have been adjusted in phase and frequency. Depending on the maximum dispersion the system is designed to allow, buffers may be required to compensate for out-of-phase signals.

A clock generator 110 receives electrical input signal d_1''' from channel ID verifier 114 and outputs an electrical signal l_1''' (Fig. 4). Clock generator 110 derives clocking information from the data resequencer portion of data resequencer/reshaper 112 that is used by a time division demultiplexing unit 108 to reconstruct the original information signal.

In accordance with still another preferred embodiment of the present invention, time division demultiplexing unit 108 provides reconstructed information electrical signals (b_1''', b_2''', b_3''', ..., b_n''') to a standard bus bridge 104 which electrically bridges the incoming bus signals onto bus/switch core backplane 86 via electrical output signals (a_1''', a_2''', a_3''', ..., a_n''') (Fig. 4) completing the network link. It is also desirable, although not mandatory that bus/switch bridge 104 be constructed to allow for transparent and asynchronous operation (both sides of bus /switch bridge 104 operate autonomously and asynchronously).

It will be appreciated by a person skilled in the art that DWDM-based transceiver network interface module 70 may be linked to a counterpart DWDM-based transceiver network interface module (not shown) via a pair of optical fibers in which case optical directional coupler 200 will be omitted and one of the optical fibers will be coupled to optical output 206 from transmitter interface 80 and the other optical fiber will be coupled to optical input 208 to complete the network link.

All of the above-identified components may be purchased commercially from various domestic or foreign electronics suppliers.

Figure 5 illustrates an example of several systems, namely systems A, B, C and D, linked with DWDM-based transceiver network interface modules. System A includes DWDM-based transceiver network interface modules 400 and 402. System B includes DWDM-based transceiver network interface modules 404 and 406. System C includes DWDM-based transceiver network interface modules 408 and 410. System D includes DWDM-based transceiver network interface modules 412 and 414. While Figure 5 demonstrates a ring topology, other topologies are possible such as point-to-point, linear, etc. Moreover, links may be unidirectional as shown by the network links between system A and B or bidirectional as shown by the network links between systems C and D.

Further details on the DWDM networking technology used in conjunction with the above-described embodiments may be found in International PCT Publication No. WO 99/35775, published on July 15, 1999, International PCT Publication No. WO 99/41863, published on August 19, 1999 and International PCT Publication No. WO 99/52232, published

on October 14, 1999, all three PCT publications incorporated herein by reference with the applicant in all three PCT patent applications being the assignee in the instant patent application.

It will be appreciated by a person skilled in the art that the present invention as described hereinabove also provides the means for building a novel fully distributed virtual communication system. The novel distributed virtual communication system operates as a single logical device, within a distance range of about 200 km between two or more physical device components. The data communication is through a single logical bus or switch fabric. The data and control signals for the bus or switch would be bridged, encoded and transmitted over one or more DWDM channels at the transmitter end and received, decoded and bridged at the receiver end. Additional DWDM channels can be utilized to create a bi-directional link between two or more system components.

It will be further appreciated by a person skilled in the art that the present invention also provides the means for utilizing one or more physical DWDM channels within a system to create a high-speed logical channel, operating at multiples of the original physical channel speeds. The inventive method provides the ability to distribute a single physical signal onto one or more logical channels, encode that signal, and transmit the encoded signal over a plurality of DWDM channels via the transmitter. At the receiver, the system receives the plurality of DWDM channels, decodes the channels and reintegrates the physical signals to recover the original signal.

While the present invention has been described in detail with regards to the preferred embodiments, it should be appreciated that various modifications and variations may be made in the present invention without departing from the scope or spirit of the invention. Various other embodiments may be possible, however, it is important to note in this regard that practicing

the invention is not limited to the applications and embodiments described herein above. Many other applications and/or alterations and embodiments may be utilized provided that they do not depart from the intended purpose of the present invention.

It should further be appreciated by a person skilled in the art that features illustrated or described as part of one embodiment can be used in another embodiment to provide yet another embodiment such that the features are not limited to the specific embodiments described above. Thus, it is intended that the present invention cover such modifications, embodiments and variations as long as they come within the scope of the appended claims and their equivalents.

What is Claimed is:

1. A dense wavelength division multiplexing-based transmitter network interface module for coupling to the internal bus/switch core backplane of a communication system, said dense wavelength division multiplexing-based transmitter network interface module comprising:

(a) a bus/switch bridge electrically coupled directly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane;

(b) a data buffer coupled electrically to said bus/switch bridge for buffering information transmitted from the bus/switch core backplane through said bus/switch bridge between bus cycles and generating a plurality of output signals;

(c) a time division multiplexing unit coupled electrically to said data buffer for receiving said output signals from said data buffer and outputting time division multiplexed output signals;

(d) at least one dense wavelength division multiplexing transmitter for receiving said time division multiplexed output signals and generating narrowband dense wavelength division multiplexing optical signals; and

(e) a dense wavelength division multiplexing multiplexer optically coupled to said at least one dense wavelength division multiplexing transmitter for receiving said narrowband optical signals and optically multiplexing said narrowband optical signals for output onto at least one optical fiber trunk in their native format.

2. The transmitter module of claim 1, further comprising:

(f) a clock generator operating in synchronism with said data buffer

(g) a channel ID generator electrically coupled to said clock generator for generating unique channel ID signals; and

(h) at least one data encoder for encoding said time division multiplexed output signals from said time division multiplexing unit with said unique channel ID signals.

3. The transmitter module of Claim 2, further comprising

(i) at least one data scrambler electrically coupled to said at least one data encoder for scrambling said encoded signals.

4. A dense wavelength division multiplexing-based receiver network interface module for coupling to the internal bus/switch core backplane of a communication system, said dense wavelength division multiplexing-based receiver network interface module comprising:

(a) a bus/switch bridge electrically coupleddirectly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane;

(b) a dense wavelength division multiplexing demultiplexer optically coupled to at least one optical fiber trunk for receiving a dense wavelength division multiplexed optical signal from said at least one optical fiber trunk and separating said received dense wavelength division multiplexed optical signal by wavelength into individual optical output signals;

(c) at least one dense wavelength division multiplexing receiver optically coupled to said dense wavelength division multiplexing demultiplexer for receiving said individual

optical output signals and converting said received individual optical output signals into corresponding electrical output signals; and

(d) a time division demultiplexing unit electrically coupled to said bus/switch bridge for reconstructing said electrical signals into their native format prior to transmission to the bus/switch core backplane through said bus/switch bridge.

5. The receiver module of Claim 4, further comprising

(f) at least one data decoder for decoding said electrical output signals from said at least one dense wavelength division multiplexing receiver;

(g) a channel ID verifier for receiving said decoded electrical signals and recovering sequencing information from said decoded electrical signals;

(h) a clock generator electrically coupled to said channel ID verifier for deriving clocking information from said verified electrical signals.

6. The dense wavelength division multiplexing-based receiver network interface module of Claim 5, further comprising

(i) at least one data unscrambler electrically coupled to said at least one data decoder for unscrambling said decoded electrical signals.

7. The dense wavelength division multiplexing-based receiver network interface module of Claim 6, further comprising

(j) a data resequencer/reshaper electrically coupled to said channel ID verifier and to said at least one data decoder and to said at least one data unscrambler, said data resequencer/reshaper electrically coupled to said time division demultiplexing unit.

8. A dense wavelength division multiplexing-based transceiver network interface module for coupling to the internal bus/switch core backplane of a communication system, said dense wavelength division multiplexing-based transceiver network interface module comprising:

a dense wavelength division multiplexing-based transmitter network interface component, said dense wavelength division multiplexing-based transmitter network interface component comprising:

a first bus/switch bridge electrically coupled directly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane;

a data buffer coupled electrically to said first bus/switch bridge for buffering information transmitted from the bus/switch core backplane through said first bus/switch bridge between bus cycles and generating output signals;

a time division multiplexing unit coupled electrically to said data buffer for receiving said output signals from said data buffer time division multiplexed output signals;

a clock generator electrically coupled to said data buffer for receiving said data buffer output signals and supplying timing information based on the speed of said data buffer output signals to said time division multiplexing unit, said time division multiplexing unit sequentially receiving said data buffer output signals and generating time division multiplexed output signals;

a channel ID generator electrically coupled to said clock generator for receiving timing information signals from said clock generator and generating unique channel ID signals;

means for encoding said time division multiplexed output signals from said time division multiplexing unit with said unique channel ID signals;

means for scrambling said encoded signals;

at least one dense wavelength division multiplexing transmitter for receiving said scrambled encoded electrical signals and generating narrowband dense wavelength division multiplexing optical signals; and

a dense wavelength division multiplexing multiplexer optically coupled to said at least one dense wavelength division multiplexing transmitter for receiving said narrowband optical signals and optically multiplexing said narrowband optical signals for output onto an optical fiber;

a dense wavelength division multiplexing-based receiver network interface component, said dense wavelength division multiplexing-based receiver network interface component comprising:

a second bus/switch bridge electrically coupled directly to the bus/switch core backplane for communicating electrically with the bus/switch core backplane;

a dense wavelength division multiplexing demultiplexer optically coupled to said optical fiber for receiving a dense wavelength division multiplexed optical signal from said optical fiber and separating said received dense wavelength division multiplexed optical signal by wavelength into individual optical output signals;

at least one dense wavelength division multiplexing receiver optically coupled to said dense wavelength division multiplexing demultiplexer for receiving said individual optical output signals and converting said received individual optical output signals into corresponding electrical output signals;

means for decoding said electrical output signals from said at least one dense wavelength division multiplexing receiver;

means for unscrambling said decoded electrical signals;

a channel ID verifier for receiving said decoded electrical signals and recovering sequencing information from said decoded electrical signals;

means for resequencing and reshaping said unscrambled decoded electrical signals from said sequencing information recovered decoded electrical signals;

a clock generator electrically coupled to said channel ID verifier for deriving clocking information from said resequenced electrical signals; and

a time division demultiplexing unit electrically coupled between said clock generator and said second bus/switch bridge for receiving clocking information from said clock generator and for reconstructing said resequenced and reshaped electrical signals, said second bus/switch bridge receiving said reconstructed electrical signals; and

an optical coupler for directionally coupling said dense wavelength division multiplexing-based transmitter network interface component and said dense wavelength division multiplexing-based receiver network interface component, said optical coupler adapted for optically coupling to said optical fiber, said optical fiber carrying at least one dense wavelength division multiplexing multiplexed optical signal in its native format.

9. A method for extending the bus/switch core of a communication system over a substantial distance, said method comprising the steps of:

(a) providing at least two dense wavelength division multiplexing-based network interface modules, each having at least one bus/switch bridge,

(b) electrically coupling the first bus/switch bridge directly to a bus/switch core backplane of the communication system; and

(c) electrically coupling the second bus/switch bridge directly to the bus/switch core backplane of a second communication system, and

(d) using a wavelength division optical fiber and a combination of dense wavelength division optical multiplexing and time division electrical multiplexing to connect the first bus/bridge to the second bus/bridge,

wherein the optical multiplexing and the electrical multiplexing is transparent to the native format of the electrical signals received from and transmitted to the bus/switch bridges.

10. The method of claim 9, further comprising the steps of

(e) encoding the time division multiplexed output signals from said time division multiplexing unit with unique channel ID signals;

(f) recovering sequencing information including said unique channel ID signals from the demultiplexed electrical signals; and

(g) using the sequencing information to reconstruct recovered the received signals in said native format.

FIGURE 1

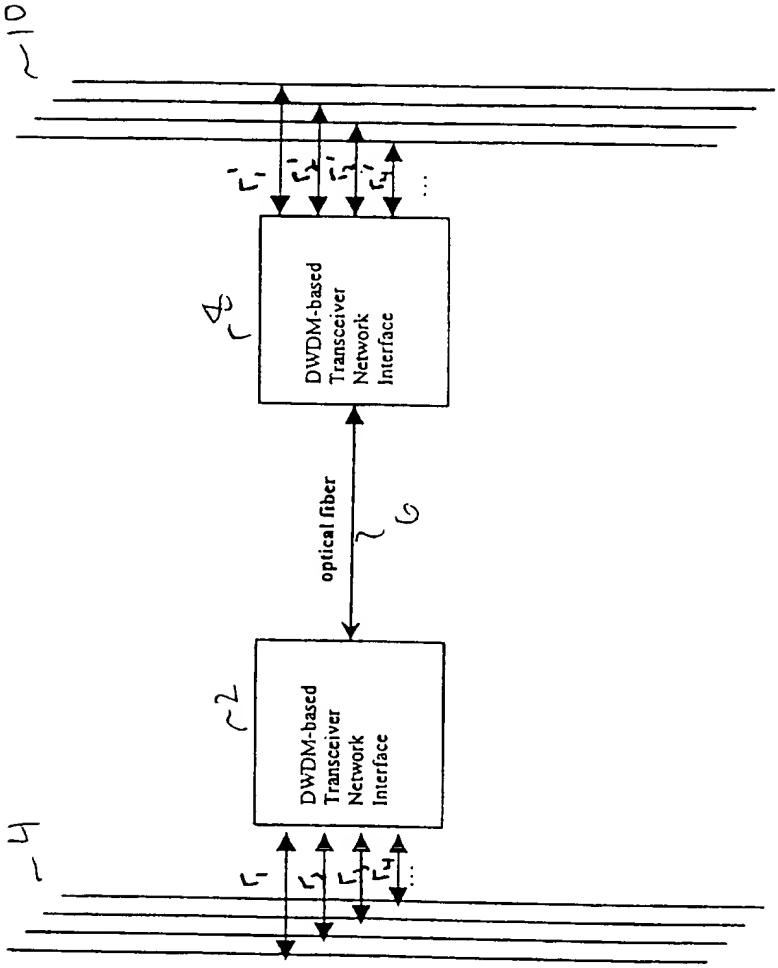
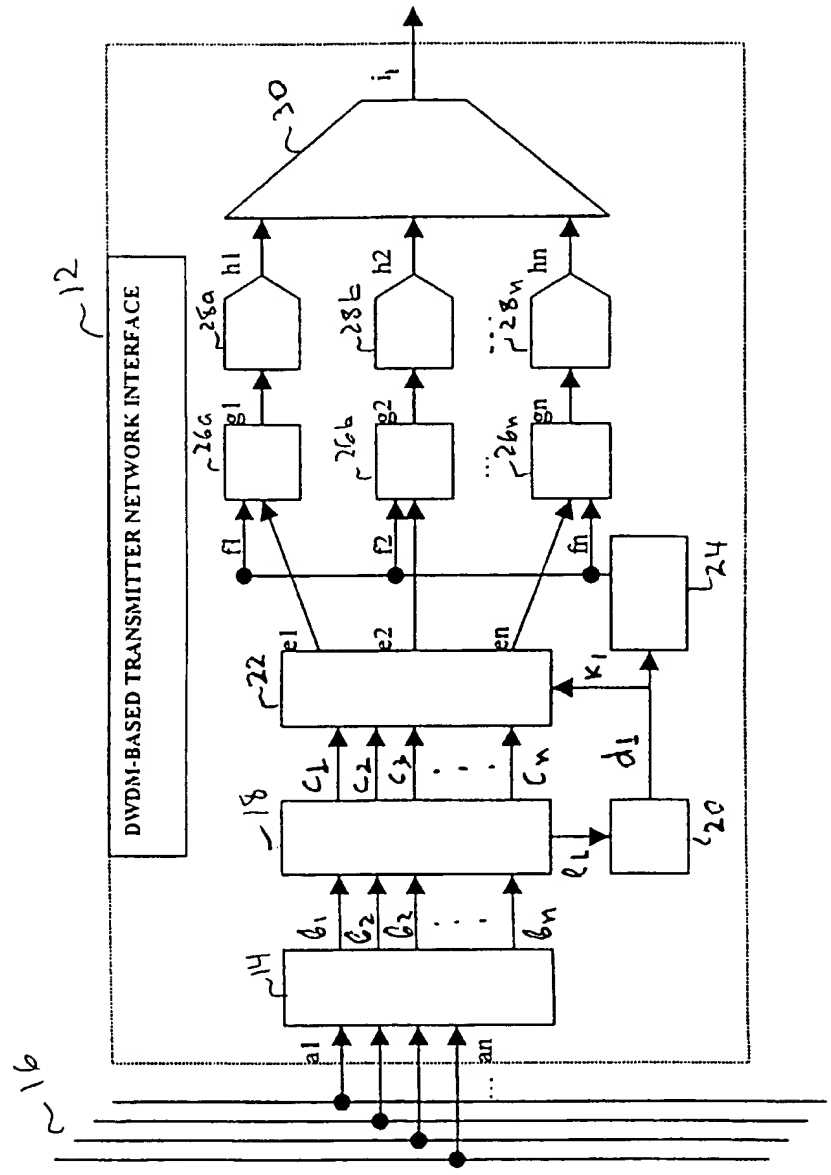

10
DWDM-based Transceiver Network Interface
4
optical fiber
6
DWDM-based Transceiver Network Interface
2
4

FIGURE 2


DWDM-BASED TRANSMITTER NETWORK INTERFACE
12
16
14
18
20
22
24
26a
26b
26n
28a
28b
28n
30
a1
an
b1
b2
b3
bn
c1
c2
c3
cn
d1
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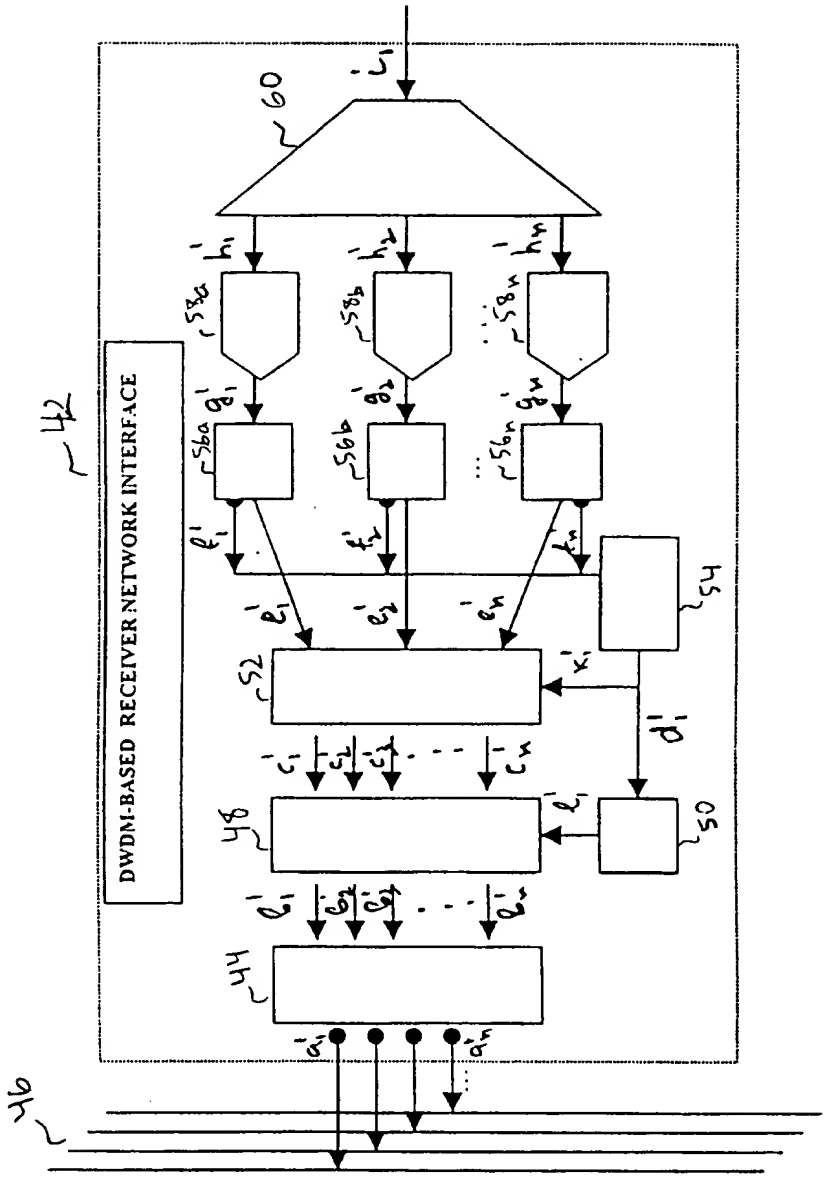
h2
hn
i1
k1
l1

FIGURE 3



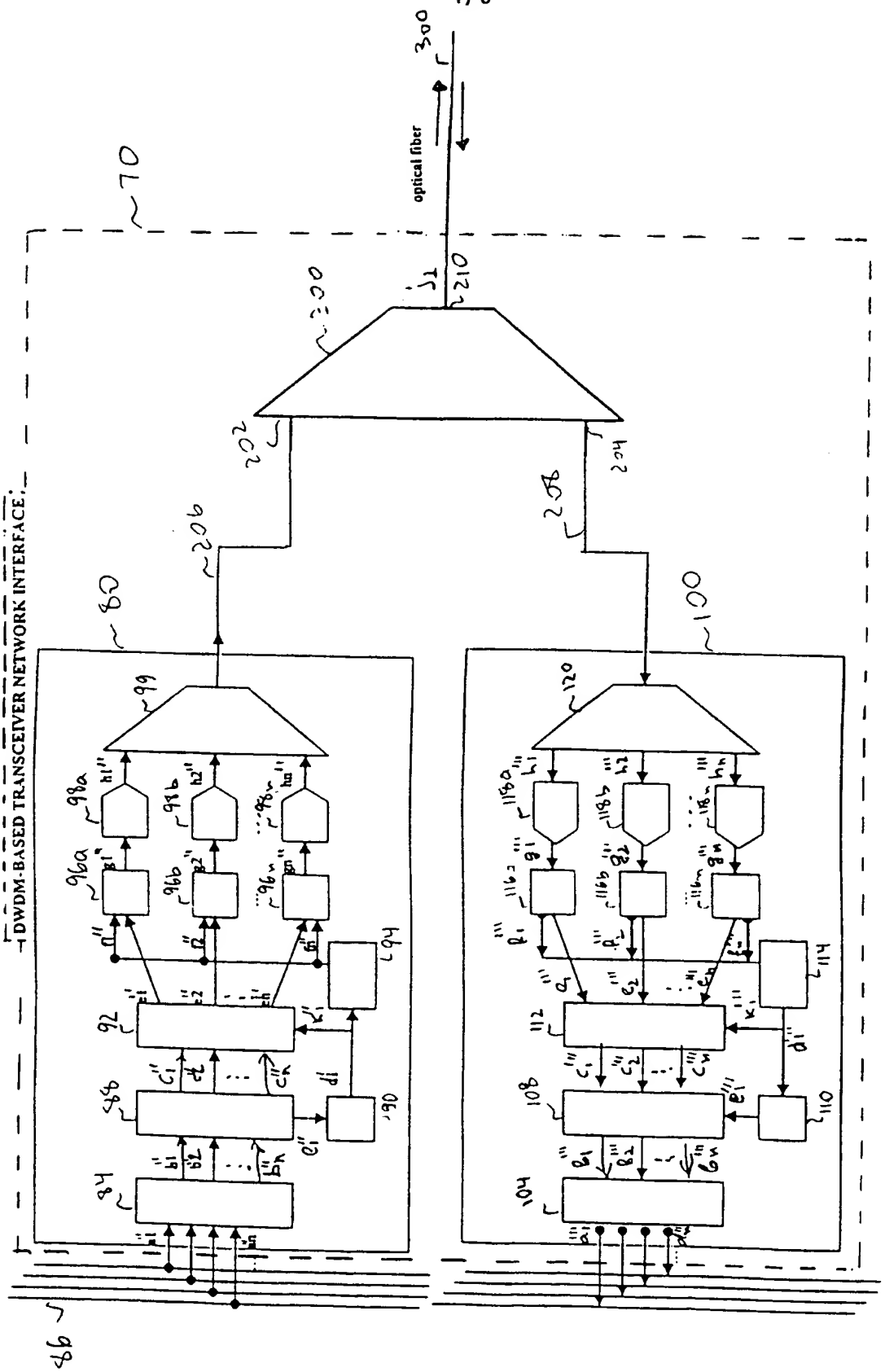


FIGURE 4

FIGURE 5

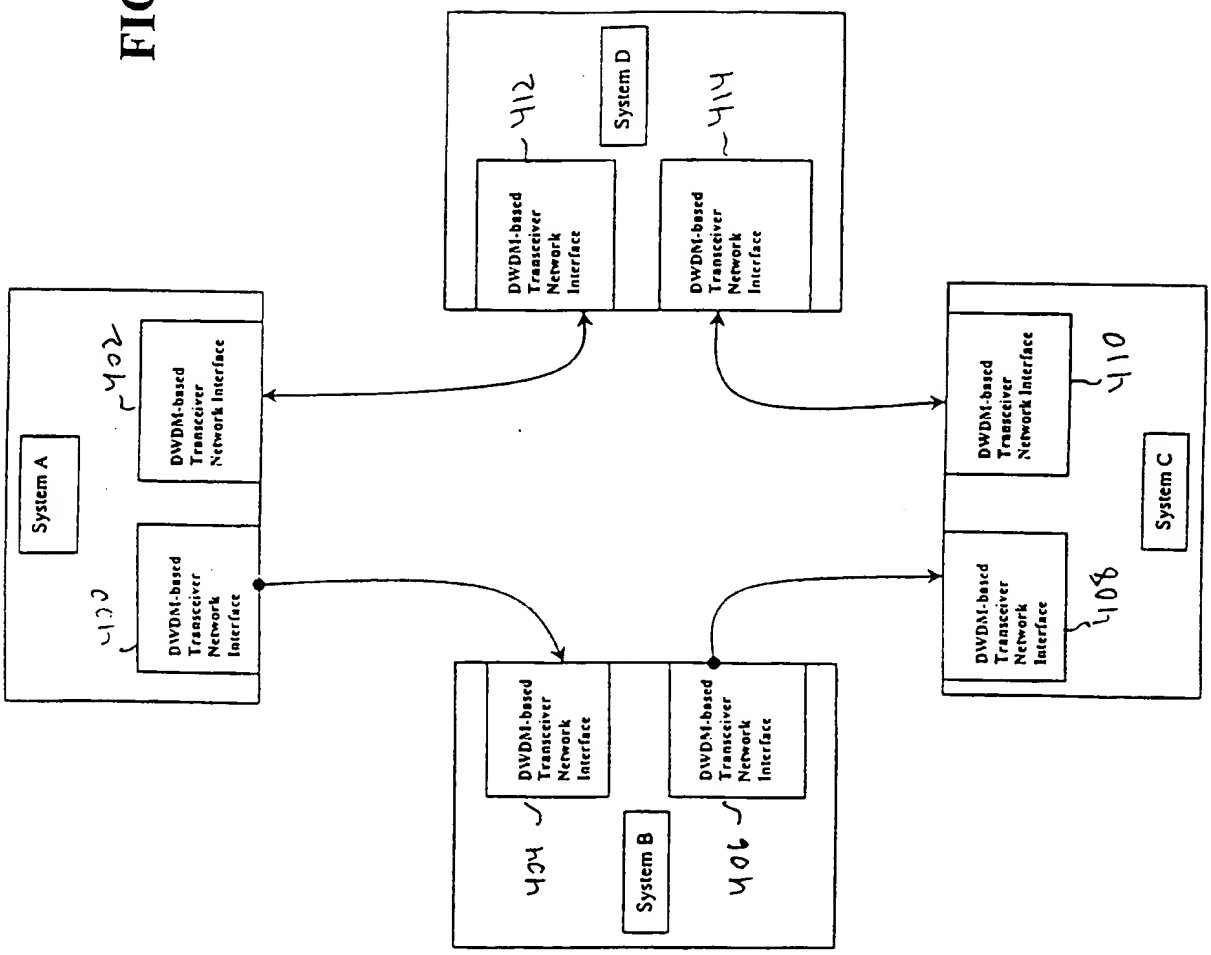
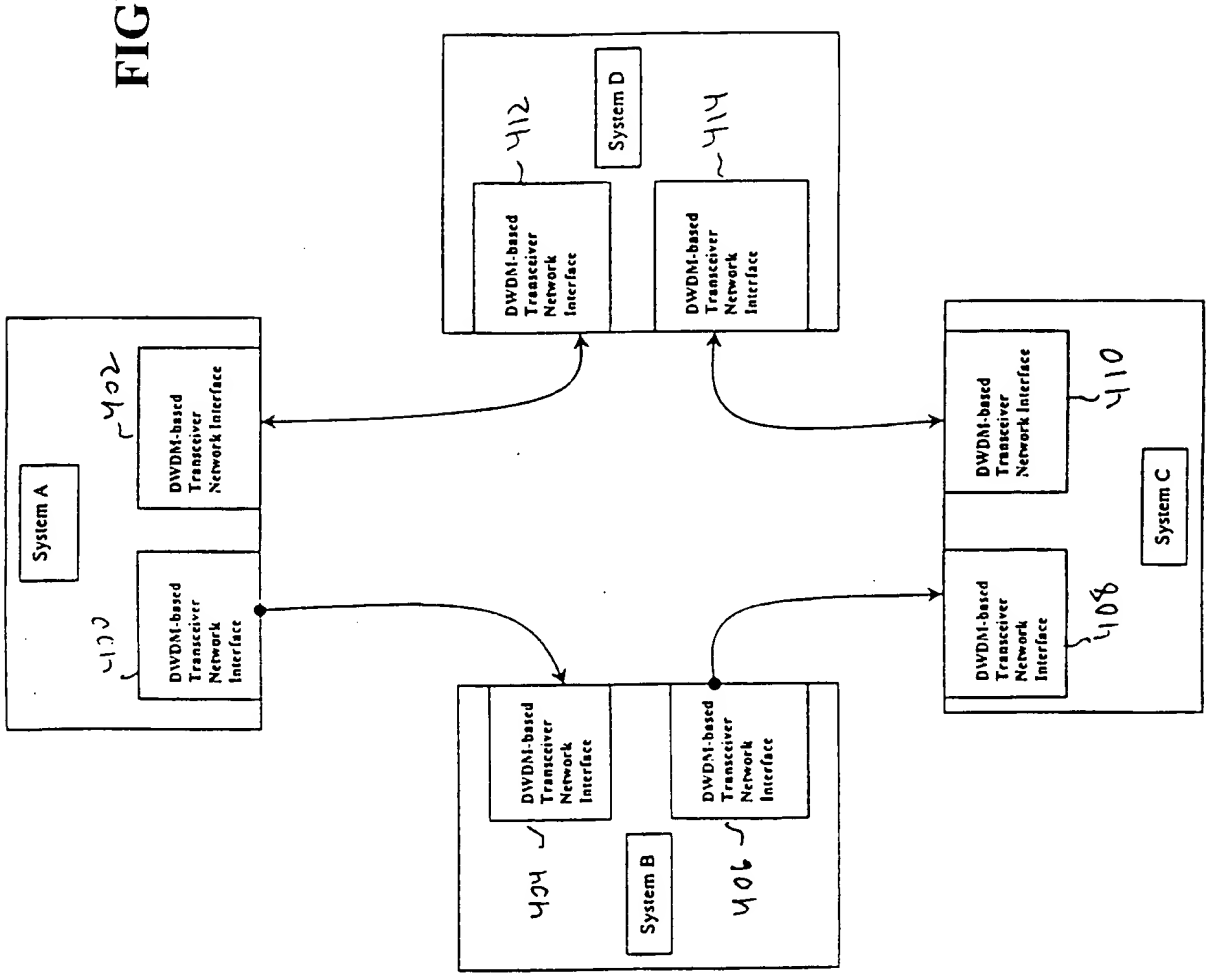

System A
DWDM-based Transceiver Network Interface
402
DWDM-based Transceiver Network Interface
400
System D
DWDM-based Transceiver Network Interface
412
DWDM-based Transceiver Network Interface
414
System C
DWDM-based Transceiver Network Interface
410
DWDM-based Transceiver Network Interface
408
System B
DWDM-based Transceiver Network Interface
404
DWDM-based Transceiver Network Interface
406

FIGURE 5


System A
DWDM-based Transceiver Network Interface
402
DWDM-based Transceiver Network Interface
System D
412
DWDM-based Transceiver Network Interface
414
DWDM-based Transceiver Network Interface
System B
404
DWDM-based Transceiver Network Interface
406
DWDM-based Transceiver Network Interface
System C
410
DWDM-based Transceiver Network Interface
408

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/11386

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04J14/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 758 170 A (NIPPON ELECTRIC CO) 12 February 1997 (1997-02-12) abstract column 3, line 16 -column 5, line 3	1-10
A	EP 0 667 690 A (IBM) 16 August 1995 (1995-08-16) abstract column 4, line 20 -column 8, line 44	1-10
A	EP 0 395 828 A (KODEN KOGYO) 7 November 1990 (1990-11-07) abstract column 4, line 34 -column 5, line 57	1-10
A	WO 99 21316 A (CIENA CORP) 29 April 1999 (1999-04-29) the whole document	1-10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 August 2000	18/08/2000

Name and mailing address of the ISA	Authorized officer
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Int onal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 99 41863 A (OSICOM TECHNOLOGIES INC) 19 August 1999 (1999-08-19) cited in the application abstract page 7, line 26 -page 14, line 5	1-10

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INTERNATIONAL SEARCH REPORT

information on patent family members

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